CLAIMS

1. A sensing device (10) for reading data stored in a passive matrix memory comprising memory cells in the form of ferroelectric capacitors, wherein said sensing device (10) senses a current response corresponding to the data, typically a binary one or a binary zero, and performs an integration of two read values,

characterized in that the sensing device (10) comprises an integrator circuit (11) for sensing the current response and means (16,17,18) for storing and comparing two consecutive read values, one of which is a reference value.

2. A sensing device (10) according to claim 1,

characterized in that the integrator circuit (1) comprises an operational amplifier (12) and a capacitor (C1) connected between an inverting input (14) of the operational amplifier (12) and the output (15) thereof.

3. A sensing device (10) according to claim 2,

characterized in that the integrator circuit comprises a switch (SW1) connected in parallel over the capacitor (C1).

4. A sensing device (10) according to claim 1,

characterized in that the means (16,17,18) for two consecutive reads comprises a first sample/hold circuit (16) for sampling/storing a first read value, a second sample/hold circuit (17) for sampling/storing a second read value, and a

comparator circuit (18) connected to the outputs of the sample/hold circuits (16;17) for determining the state of an addressed memory cell.

5. A sensing device (10) according to claim 4, characterized in that the sample/hold circuits (16;17) comprise capacitors (C_2;C_3).

6. A sensing device (10) according to claim 4, characterized in that the comparator circuit (18) is an operational amplifier.

7. A sensing device (10) according to claim 4 characterized in that a correction circuit (21) is connected between the second sample/hold circuit (17) and the output (15) of the integrator circuit (11).

8. A read method for use with the sensing device according to claim 1, wherein the sensing device are used for reading data stored in a passive matrix memory with word and bit lines and comprising memory cells in the form of ferroelectric capacitors at crossings between the word and bit lines, wherein the sensing device senses a current response corresponding to the data stored in a memory cell, typically at binary one or a binary zero, and performs an integration of read values, wherein the read method comprises controlling the electric potentials on all word and bit lines in time latching word line potentials to potentials selected among predetermined word line potentials and either latching bit lines to potentials selected among predetermined bit line potentials,

wherein bit lines in a read cycle are connected to the sensing device for sensing a charge flowing between a selected bit line and a memory cell at the crossing of the former and a word line activated by being latched to a selected potential for initializing the read cycle,

characterized by performing two consecutive reads of a memory cell, integrating each read over a predetermined time period respectively to generate a first and a second read value, storing said read values, comparing the stored read values, and determining a logical value dependent on the sensed charge.

9. A read method according to claim 8,

characterized by introducing a time delay between two consecutive reads in a read cycle.

add B3